

TC74HC107AP, TC74HC107AF, TC74HC107AFN

(Note) The JEDEC SOP (FN) is not available in Japan.

DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC107A is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

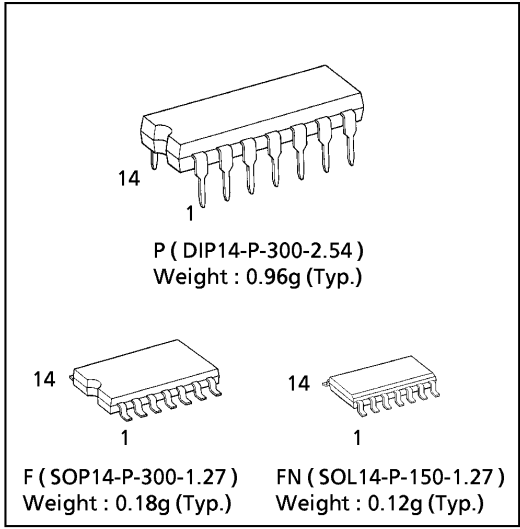
In accordance with the logic levels applied to the J and K inputs, the outputs change state on the negative going transition of the clock pulse.

$\overline{\text{CLR}}$ is independent of the clock and is accomplished by a low logic level on the input.

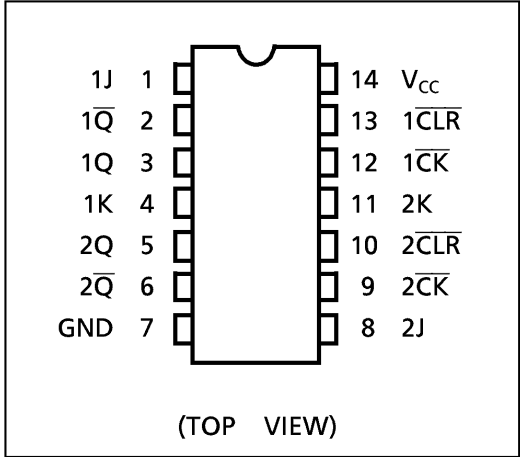
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $f_{\text{MAX}} = 75\text{MHz}$ (typ.)
at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 2\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (Min.)
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{\text{OH}}| = I_{\text{OL}} = 4\text{mA}$ (Min.)
- Balanced Propagation Delays..... $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide Operating Voltage Range... V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS107



PIN ASSIGNMENT

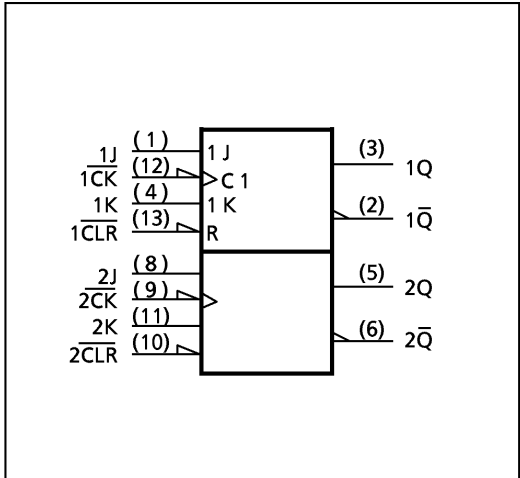


TRUTH TABLE

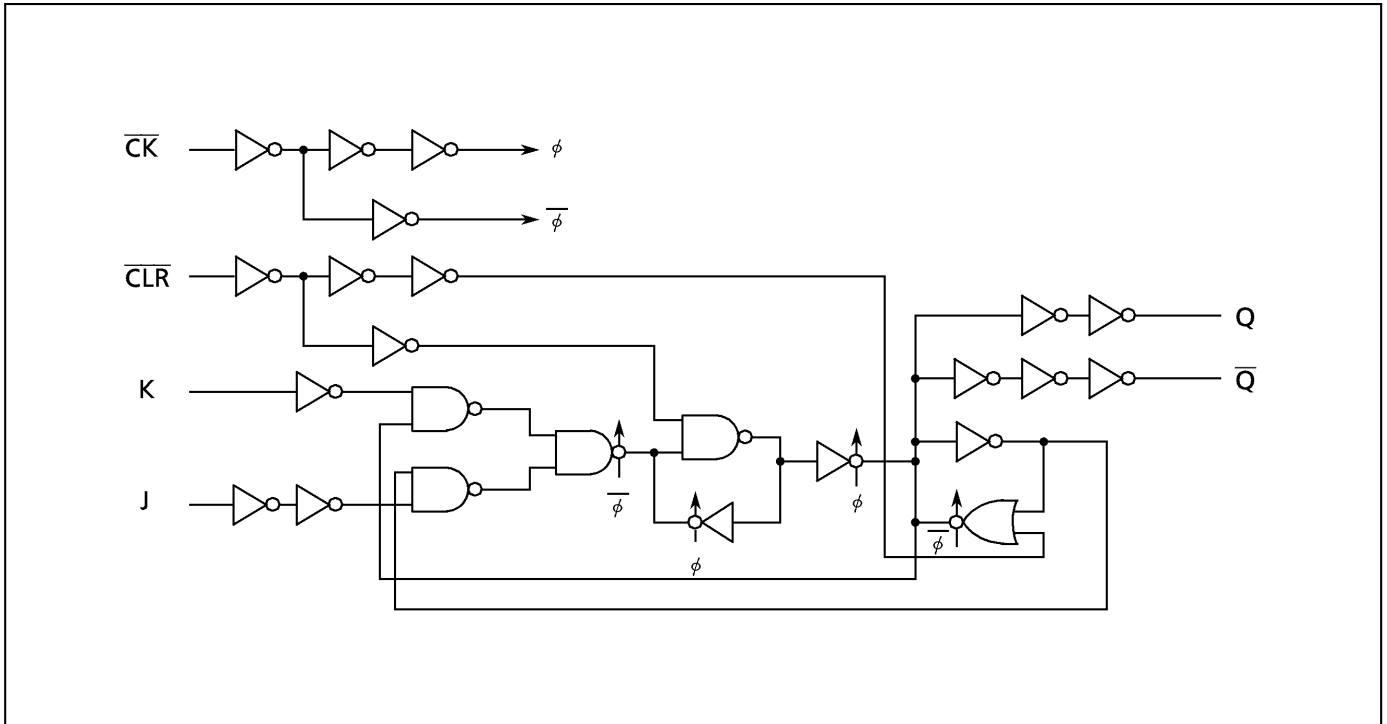
INPUTS				OUTPUTS		FUNCTION
CLR	J	K	CK	Q	Q-bar	
L	X	X	X	L	H	CLEAR
H	L	L	\downarrow	Q_n	\overline{Q}_n	NO CHANGE
H	L	H	\downarrow	L	H	—
H	H	L	\downarrow	H	L	—
H	H	H	\downarrow	\overline{Q}_n	Q_n	TOGGLE
H	X	X	\uparrow	Q_n	\overline{Q}_n	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0\text{V}$) 0~500 ($V_{CC} = 4.5\text{V}$) 0~400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0	μA	
			6.0	—	—	2.0	—	20.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	2.0	—	20.0	μA	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLR)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time (CLR)	t_{rem}		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	37	30	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH}		—	4	8	ns
	t_{THL}					
Propagation Delay Time (CK-Q, Q)	t_{PLH}		—	11	21	
	t_{PHL}					
Propagation Delay Time (CLR-Q, Q)	t_{PLH}		—	12	24	
	t_{PHL}					
Maximum Clock Frequency	f_{MAX}		34	75	—	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (CK-Q, Q)	t_{PLH} t_{PHL}		2.0	—	48	125	—	155	
			4.5	—	14	25	—	31	
			6.0	—	12	21	—	26	
Propagation Delay Time (CLR-Q, Q)	t_{PLH} t_{PHL}		2.0	—	52	140	—	175	
			4.5	—	15	28	—	35	
			6.0	—	13	24	—	30	
Maximum Clock Frequency	f_{MAX}		2.0	6	23	—	5	—	MHz
			4.5	31	70	—	25	—	
			6.0	37	80	—	30	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			—	33	—	—	—	

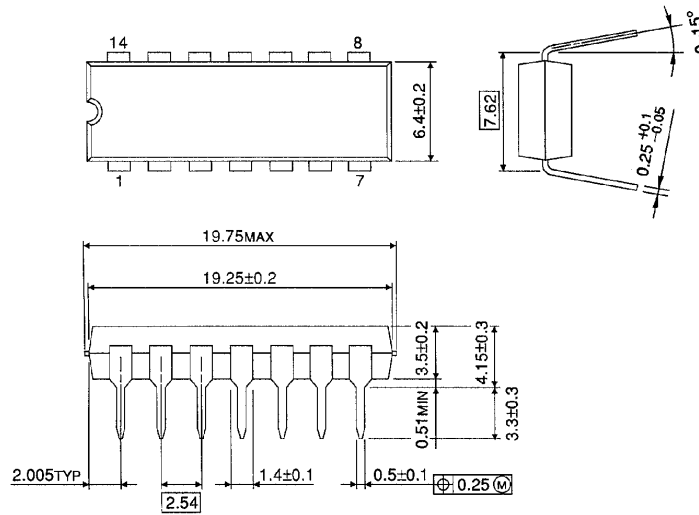
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per F / F)}$$

DIP 14PIN PACKAGE DIMENSIONS (DIP14-P-300-2.54)

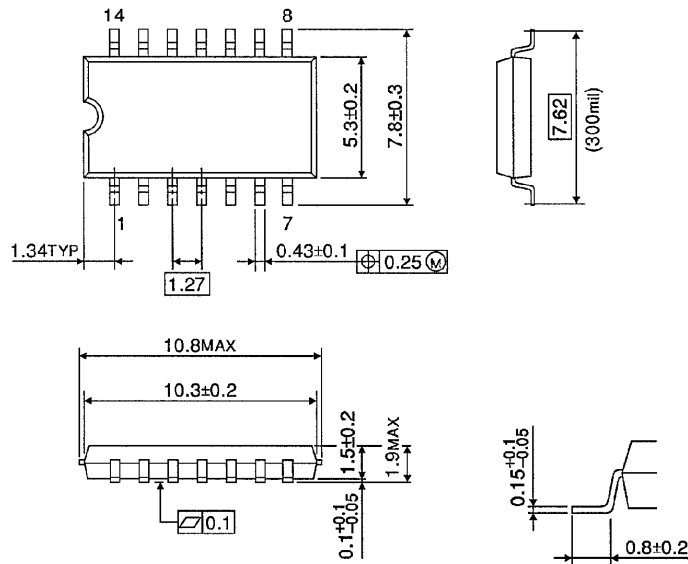
Unit in mm



Weight : 0.96g (Typ.)

SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm

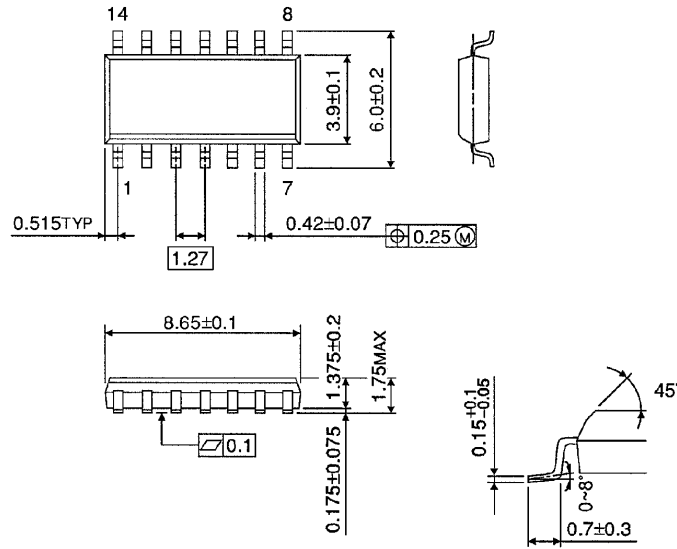


Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOL14-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

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